Design and Performance Analysis of Encoders using Reversible logic gates

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ABSTRACT: Reversible logic gates are very interesting topic for research due to less heat dissipation and low power consumption. Reversible logic gates are used in various applications such as CMOS design, Quantum computing, Nanotechnology, Cryptography, Optical computing, DNA computing, Digital signal processing (DSP), Communication computer graphics. Quantum computing is not realized without implementation of reversible logic .Main purposes of designing of reversible logic gates are to decrease quantum cost, garbage output, no. of gates. In this paper we present a proposed design of Encoder using Feynman and Fredkin reversible logic gates.

Keywords: Reversibility, Reversible logic gates, Quantum cost, Garbage output.

1. INTRODUCTION

Reversibility in computing implies that information about the computational states should never be lost. The information can be recovered for any earlier stage by computing backwards or un-computing the results. This is termed as "logically reversibility". Physical reversibility is a process that dissipates no heat in terms of wastage of energy [1]. Power dissipation of reversible circuit, under ideal physical circumstances, is zero. The loss of information is associated with laws of physics describing that one bit of information lost dissipates kTln2 of energy, where k is Boltzmann' constant and T is the temperature of the system [2]. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits. To increase the portability of devices again, reversible computing is required.

Reversible are circuits or gates that have one to one mapping between vectors of inputs and outputs, thus the vector of input states can be always reconstructed from the vector of output states. In reversible logic gates the number of output bits always equals the number of input bits. The fan out of every signal including primary inputs in a reversible gate must be one.

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Figure1: A reversible gate with n-inputs and n-outputs is called n*n gate.

1.1 ORGANIZATION OF WORK

This section describes the organization of the paper. Section 1 includes the introduction of reversibility. Section 2 shows the Literature Review. Section 3 describes different types of reversible logic gates. Section 4 includes different parameters of reversible logic gates. Section 5 includes the proposed work. Section 6 includes results and discussions Section 7 includes conclusion with future scope. References are shown in next section.

2. LITERATURE SURVEY

In 2008, Majid Mohammadi et.al explained quantum gates uses in implementation of binary reversible logic circuits. They proposed behavioral models for well known V & V+ quantum gates. They explained that their proposed representation is used to synthesize reversible logic circuits instead of the known unitary matrix form of quantum gates [3].

In march 2010,D.Michel miller et.al. explained that one approach to determining a quantum circuit is to first synthesize a circuit composed of binary reversible gates and to then map that circuit to an equivalent quantum gate realization. In this paper they were considered that mapping phase with the goal of reducing the no. Of quantum gates required. They were presented the results for quantum library for NOT, Controlled NOT and square root of NOT gate[4].

In 2011,Prof. Suiata S.Chiwande et.al. presented a basic reversible gate to build complicated circuits which can be implemented in some sequential circuits as well as in some combinational circuits. They also built adder circuits using

basic gates like Peres and TSG gate. They also proposed 4-bit reversible asynchronous down counter and explained that this counter is used in applications of digital circuits like timer/counter, building ALU and reversible processor[5]

In April 2012, B.Ragh Kanth et.al. compared conventional and reversible logic gates. They also realized the addition and subtraction operations using reversible DKG gate and also compared it with conventional logic gates. The author explained that a 4*4 reversible DKG gate can work singly as a reversible full adder and a reversible full subtractor.The author also compared the results of conventional adder with reversible on Xilinx 9.1 software [6].

In May 2012, Mr. Devendra Goyal et.al. Explained that reversible logic is very essential for the construction of low power, low loss computational structures which are every essentials for construction of arithmetic circuits used in quantum computation and other low power digital circuits. In this paper, they were presented the combinational circuits of all basic reversible logic gates and also had done VHDL codes of these circuits [7].

In March 2013, Raghava Garipelly et.al. explained that quantum networks composed of quantum logic gates each gate performing an elementary unitary operation on one or more two-state quantum system called qubits. They were also explained constraints for reversible logic circuits that reversible logic gates do not allow fan out and required minimum no. Of garbage outputs, constant input and also minimum quantum cost. They were proposed new 6*6 BSCL reversible logic gates.[8].

In 2014,Neeta Pandey et.al,proposed 2:4 reversible decoder and 3:8 reversible decoder using Feynman and Fredkin gate. They also implemented Feynman and Fredkin gate using transmission gates. They were also compared the various parameters of proposed decoders with exiting decoders [9].

In july 2014, Ashima Malhotra, et.al, proposed different types of reversible multiplexers using modified Fredkin gate. They were proposed 2:1,4:1,8:1 and 16:1 reversible multiplexers. They were also compared with quantum cost and power consumption of proposed reversible multiplexers with exiting one [10].

In july 2014, Ashima Malhotra, et.al, described that reversible modified Fredkin gate used to designed multiplexers. They also compared the quantum cost of multiplexers designed using Fredkin gate with multiplexers designed using modified Fredkin gate[11].

3. Different Types of Reversible Logic Gates

- NOT Gate: It is 1*1 simplest reversible logic gate with input A and output P= NOT A. The quantum cost of NOT is zero.

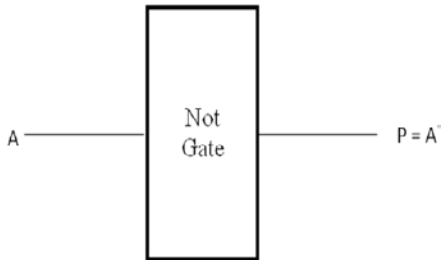

Figure 2: Symbol of NOT Gate.

- Feynman Gate: It is 2*2 reversible logic gate with inputs A & B and outputs P=A &.Q=A⊕B. The quantum cost of Feynman gate is 1.

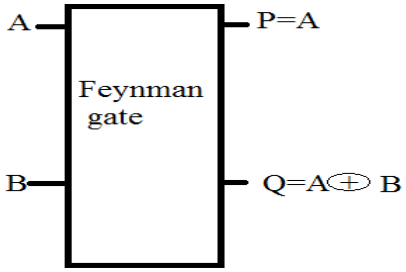

Figure 3: Symbol of Feynman Gate.

- Fredkin Gate: It is 3*3 reversible logic gates with inputs A,B,C and outputs P=A,Q=A'B+AC,R=AB+A'C. The quantum cost of Fredkin gate is 5.

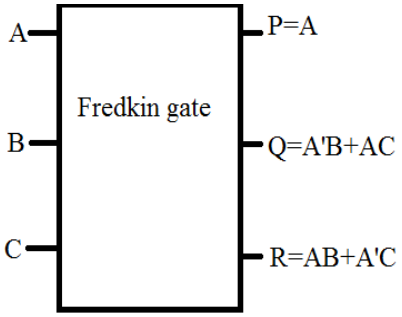

Figure 4: Symbol of Fredkin Gate.

- Toffoli Gate: It is 3*3 gate with inputs A, B, C and outputs P=A, Q=B ,R=AB⊕C. It has quantum cost 5.

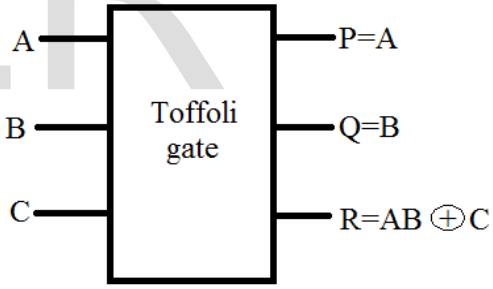

Figure 5: Symbol of Toffoli Gate.

- Peres Gate: It is 3*3 gate with inputs A, B, C and outputs P=A,Q=A⊕B ,R=AB⊕ C.It has quantum cost 4.

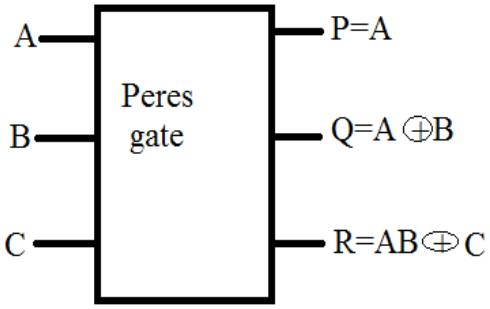

Figure 6: Symbol of Peres Gate.

4. Various Parameters for determining the performance of the circuit:

No. of Reversible Gates (N): The no. of reversible gates used in circuit.

No. of Constant Inputs (CI): The no. of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.

No. of Garbage Outputs (GO): The no. of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

Quantum cost (QC): This refers to the cost of circuit in terms of cost of primitive gates. It is calculated knowing the no. of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

5. Proposed Work:

(i) 4:2 Reversible Encoder:

The proposed 4:2 Reversible Encoder is shown in figure. It uses three Feynman gates(FG) and one Fredkin gate(FRG).It has four inputs A,B,C,D and two outputs Y1&Y2 and also has two garbage outputs g1&g2.The operation of circuit is given in Table. This proposed 4:2 Encoder has Quantum cost of 8.

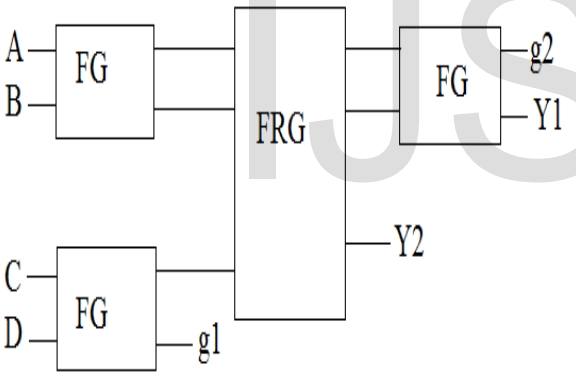

Figure7: Proposed 4:2 Reversible Encoder.

INPUTS				OUTPUTS	
A	B	C	D	Y1	Y2
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Table1: Truth table of proposed 4:2 Reversible Encoder.

(ii) 8:3 Reversible Encoder:

The proposed 8:3 Reversible Encoder is shown in figure.

It uses nine Feynman gates(FG) and two Fredkin gate(FRG).It has eight inputs A,B,C,D,E,F,G,H and three outputs Y1,Y2&Y3 and also has five garbage outputs g1,g2,g3,g4&g5.The operation of circuit is given in Table. This proposed 8:3Encoder has Quantum cost of 19.

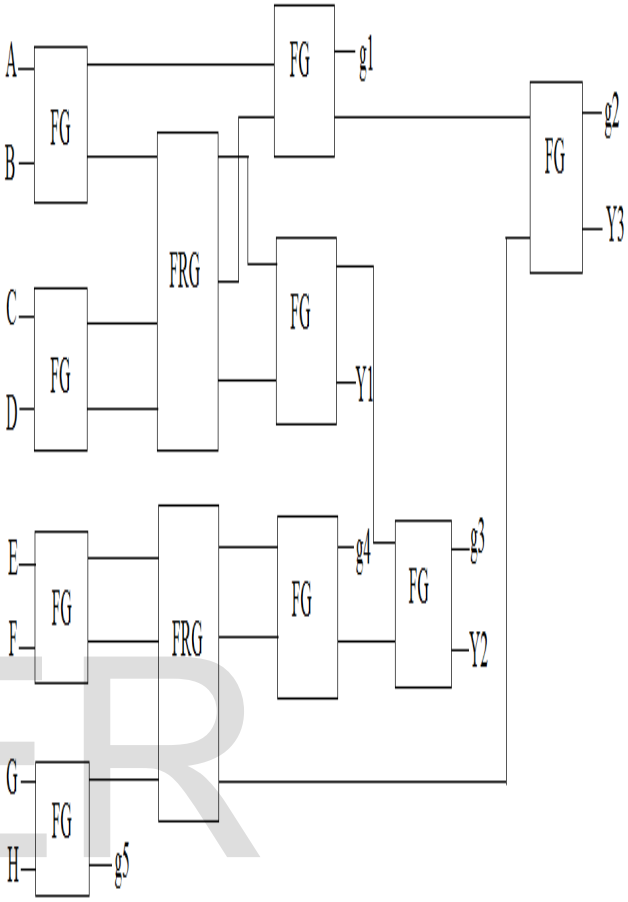

Figure8: Proposed 8:3 Reversible Encoder.

INPUTS								OUTPUTS		
A	B	C	D	E	F	G	H	Y1	Y2	Y3
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Table2: Truth table of Proposed 8:3 Reversible Encoder.

(iii) 16:4 Reversible Encoder:

The proposed 16:4 Reversible Encoder is shown in figure. It uses twenty three Feynman gates(FG) and five Fredkin gate(FRG).It has sixteen inputs A,B,C,D,E,F,G,H,I,J,K,L,M,N,O,P and four outputs Y1,Y2,Y3&Y4 and also has 12 garbage outputs g1,g2,g3,g4,g5,g6,g7,g8,g9,g10,g11,g12.The operation of circuit is given in Table. This proposed 16:4 Encoder has Quantum cost of 48.

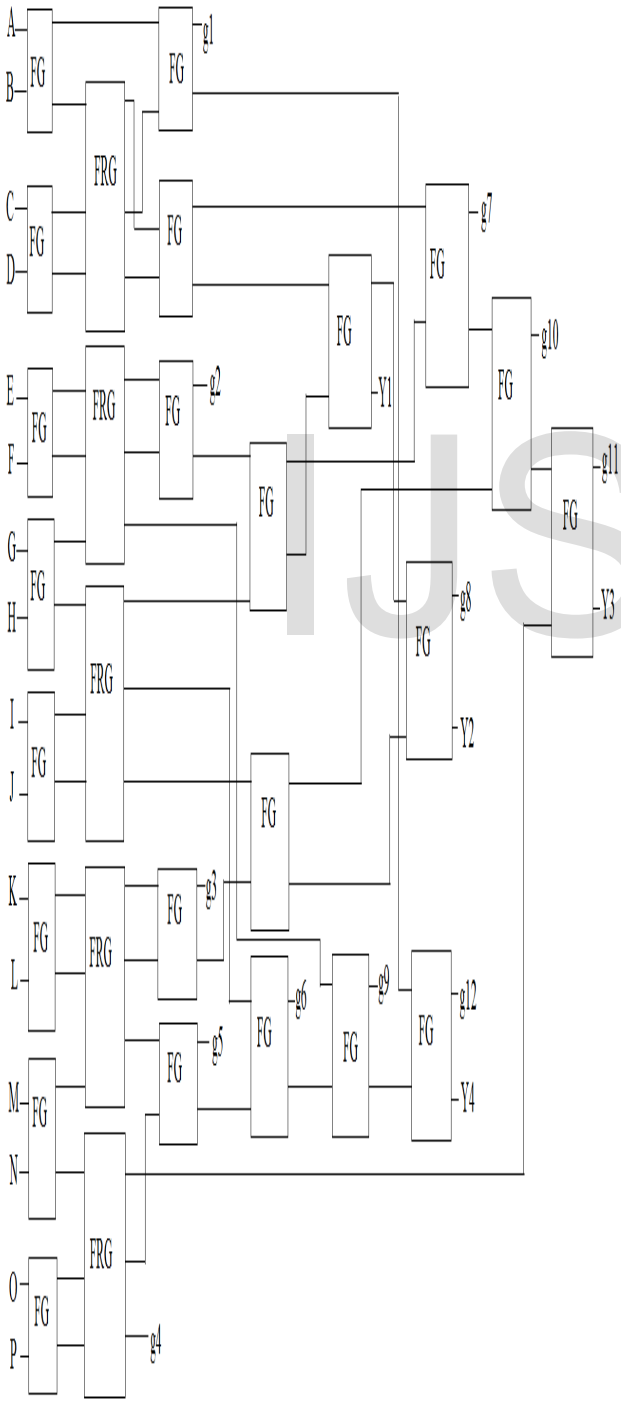

Figure9: Proposed 16:4 Reversible Encoder.

INPUTS																OUTPUTS			
A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Y1	Y2	Y3	Y4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Table3: Truth table of Proposed 16:4 Reversible Encoder.

6. SIMULATION RESULTS:

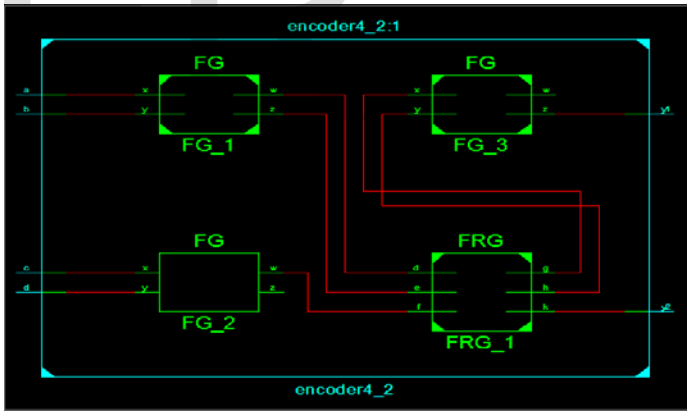

Figure10: RTL view of 4:2 Reversible Encoder.

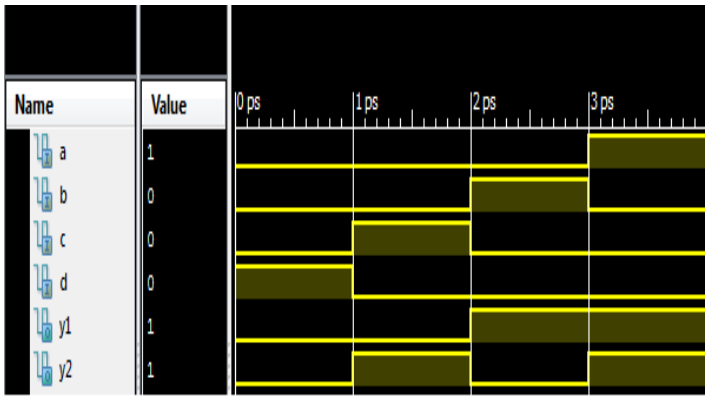

Figure11: Waveforms of 4:2 Reversible Encoder.

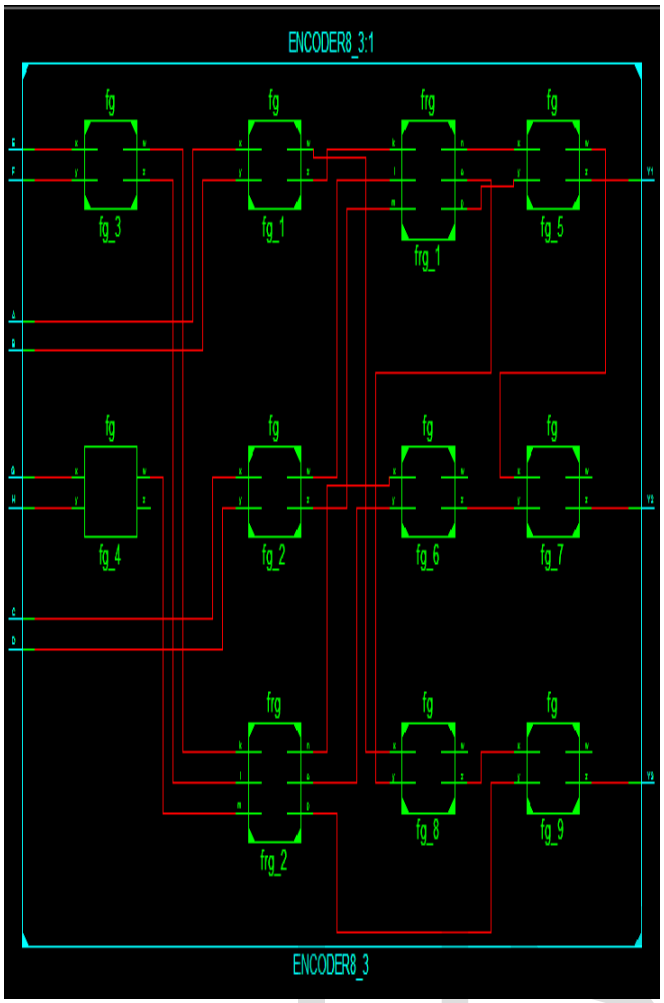

Figure12: RTL view of 8:3 Reversible Encoder.

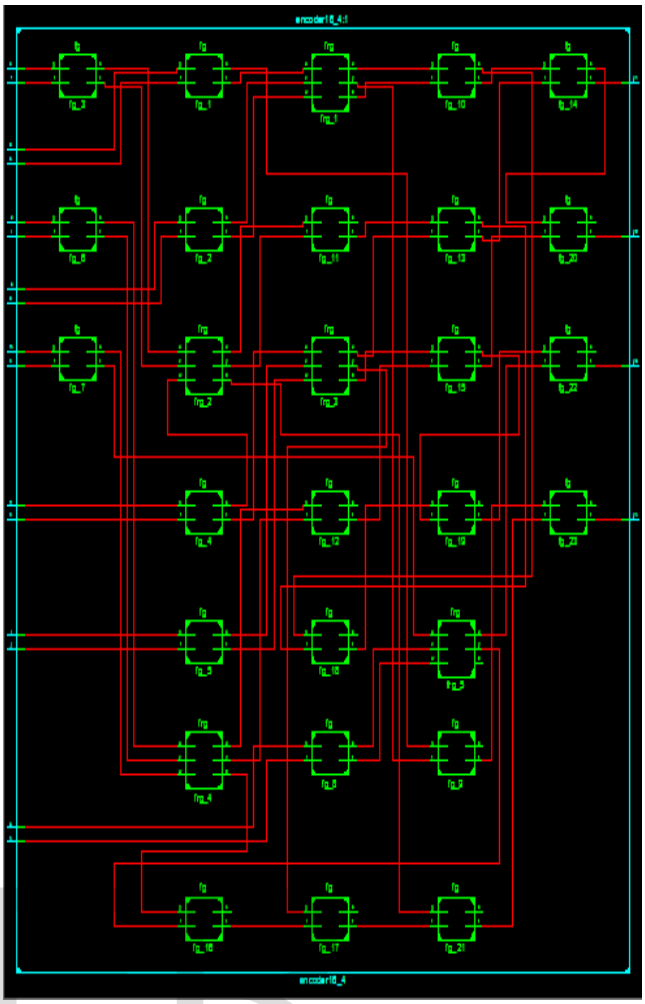

Figure14: RTL view of 16:4 Reversible Encoder.

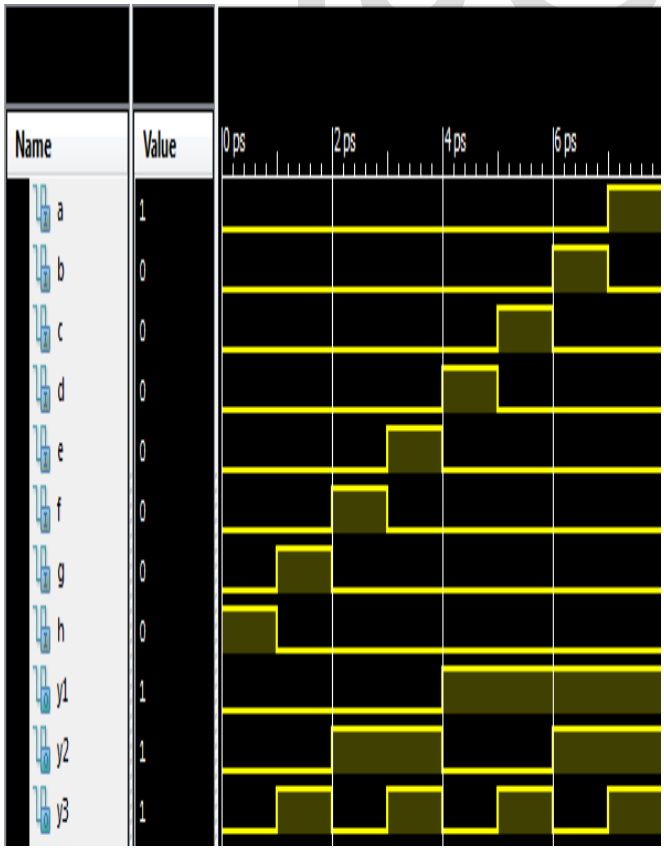

Figure13: Waveforms of 8:3 reversible Encoder.

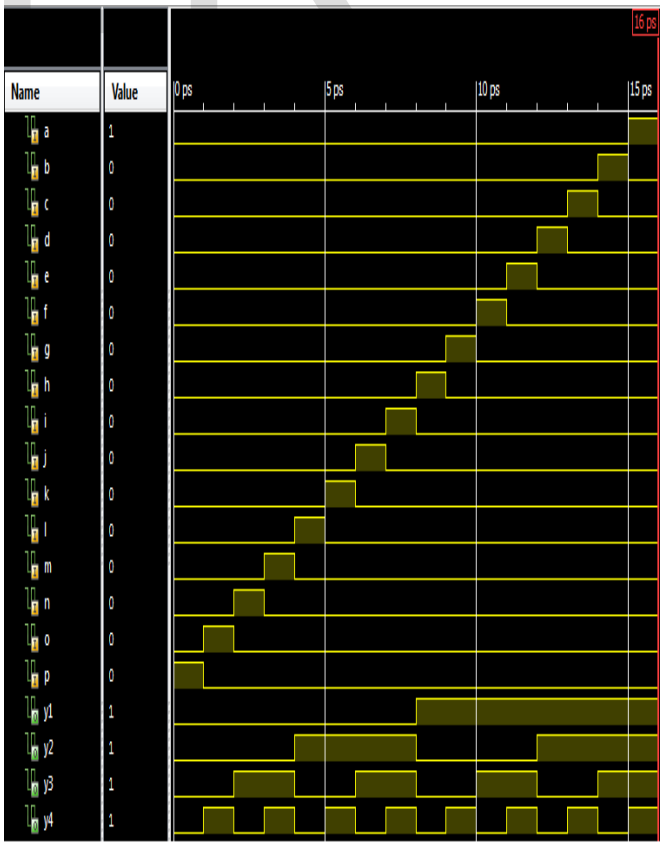

Figure15: Waveforms of 16:4 Reversible Encoder.

7. CONCLUSION AND FUTURE SCOPE

In this paper, we presented different types of reversible Encoder using Feynman and Fredkin gates.In this paper we have calculate Quantum cost of different types of reversible encoders .Quantum cost of 4:2,8:3 and 16:4 reversible encoder is 8,19 and 48 respectively. They are used in various fields such low power VLSI design, optical computing, Nanotechnology, Quantum computer, Design of low power arithmetic and data path for digital signal processing (DSP).

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